Help Volume

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Toolsets: Serial Analysis Tool

Using the Serial Analysis Tool

The Serial Analysis tool is used by digital design teams to convert streams of serial data into parallel words. Parallel word width is selectable up to 32 bits and can be displayed in a number of numeric bases. Advanced options allow you to look at a serial data stream that has no clock and to specify frames of data that have a start and end pattern, or frames ending after a specified number of bits.

Getting Started

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"Triggering on a Serial Pattern" on page 43

Using Multiple Serial Analysis Tools (see page 11)

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Glossary of Terms (see page 53)

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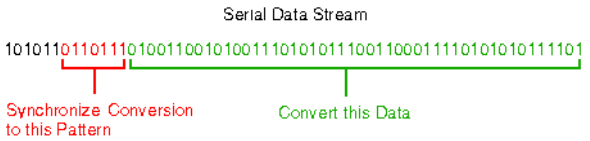
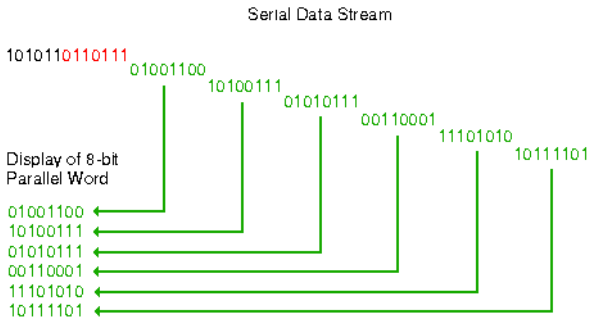
Using the Serial Analysis Tool

Overview of a Serial to Parallel Conversion

Serial to parallel conversion is used by digital design teams to convert long streams of serial data into parallel words which are easier to view and analyze. Another important element in the conversion of serial data is the ability to find specific bit patterns which identify the starting point of new data or the point where data changes. Identifying and using serial bit patterns to synchronize the start of data conversion allows the engineer to view and analyze only the desired data.



Once the data is converted, it is displayed in parallel words. For analysis purposes, it is important to be able to view words in variable lengths and in an order of least significant bit (LSB) first, or most significant bit (MSB) first.



For More Information For a conceptual example of using the Serial to Parallel tool, refer to: “Example - Using the Serial Analysis Tool” on page 7

Example - Using the Serial Analysis Tool

In most serial to parallel conversions you run the logic analyzer to acquire the serial data, then apply a serial analysis configuration to reformat the data. The resulting conversion is displayed in the Listing Display tool.

NOTE: The example shown below is intended to illustrate the general concepts of a serial to parallel conversion. Although not required, the *Credit Card Demo Board* (see page 8) can be used to provide real data for this example.

Workspace and Analyzer Setup

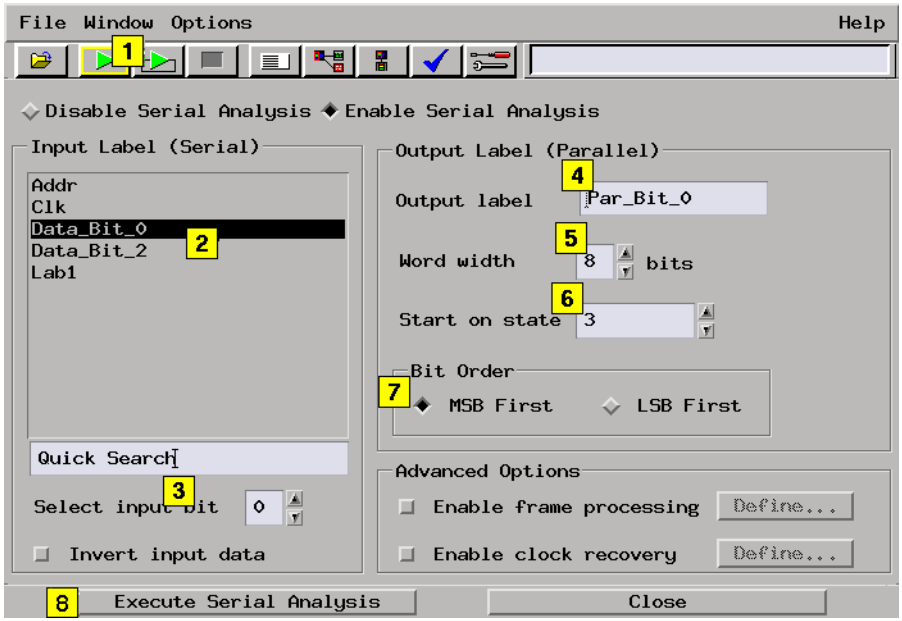
1. Configure the workspace (see page 11) with the appropriate tools.
2. Configure the logic analyzer (see page 13).
3. Connect the probing (see page 15) to your target circuit and map the probe channels (see page 17) into the Format window of the logic analyzer.

Applying a Serial to Parallel Configuration

When you execute a serial to parallel conversion, the configuration is applied to the data captured in analyzer memory. If you change the configuration, you must execute the conversion again. Also, you must re-run the analyzer if you want to update the data in analyzer memory.

1. Run the logic analyzer to acquire the serial data stream.
2. Select the input label (see page 47) containing the desired serial data from the logic analyzer. If you have multiple labels, use the *quick search* by typing the label name.
3. Select the assigned bit that the serial data is on.
4. Enter a new output label name to contain the converted parallel data.
5. Assign a width to the new parallel word.
6. Select the beginning serial sample (see page 49) where the conversion will start.

7. Select how you want the bit order (see page 48) in the new parallel word.
8. Select *Execute Serial Analysis*.
   - Any time you change the configuration, re-execute the conversion.
   - If you want new serial data, re-run the analyzer.
9. Open the Listing Display tool to view the converted data.



See Also

"Clock Recovery - Serial Data without a Clock" on page 26

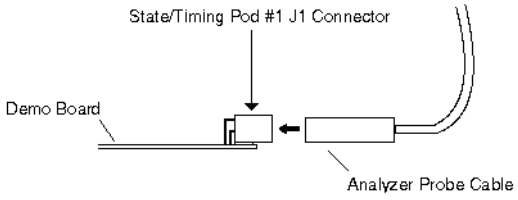
"Overview of a Serial to Parallel Conversion" on page 6

Using the Credit Card Demo Board

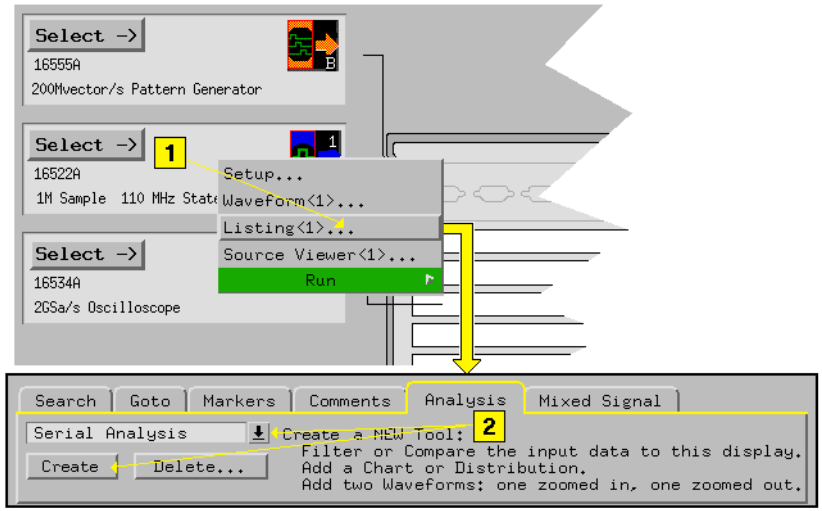
The Credit Card Demo Board is included in the *Logic Analyzer Training Kit* shipped with the logic analyzer. If you intend to use the Credit Card Demo Board, use the following workspace and analyzer setup, then go back to *Applying a Serial to Parallel Configuration.*

Connecting the Demo Board

Connect the analyzer's pod 1 cable directly into the *State/Timing Pod #1* J1 connector.

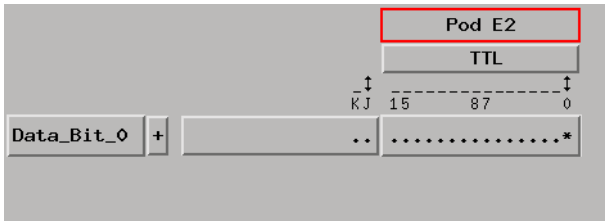


Configure the Workspace



Mapping the Data Channel into the Interface

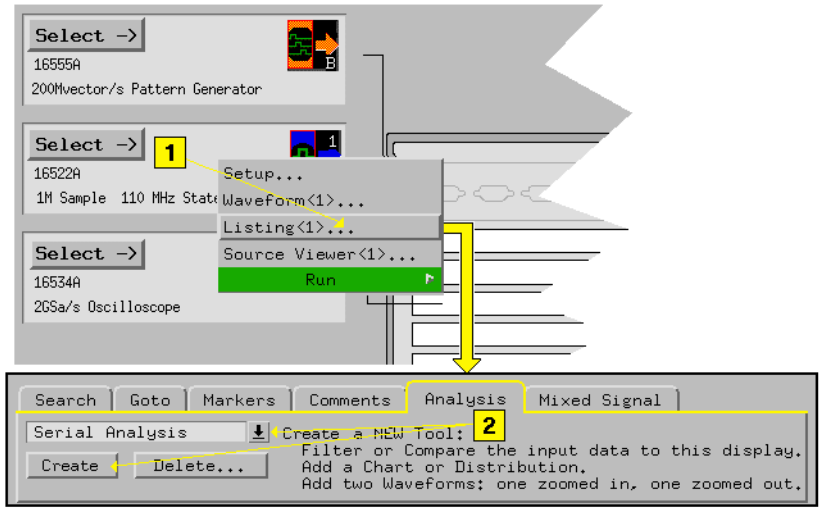
In the logic analyzer's Format window, assign bit 0 of pod 1. Turn off all other bits. In this example the label name is changed to *Data_Bit_0*.


Pod E2
TTL
KJ
15
87
0
Data_Bit_0
+
..
.....*

Workspace Configuration

Typical Single Tool Application

How you configure the workspace for a Serial to Parallel conversion may vary. However, the minimum workspace configuration includes a logic analyzer, the Serial Analysis tool, and one Listing Display tool.

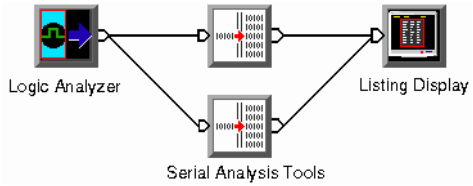


Typical Parallel Tools Application

If your application requires you to convert and view multiple serial segments, or minor frames of data within a major frame, all from the same serial data stream, use multiple Serial Analysis tools. In the Listing Display tool, simply insert the desired labels created in the multiple Serial Analysis tools.

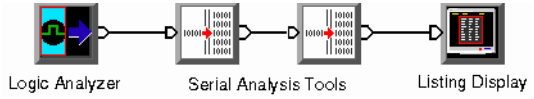
Examples of these applications are:

- To view both SEND and RECEIVE data.
- To view multiple serial lines simultaneously.
- Using the *Pass selected bits in data block* feature to view selected words within the same frame.



Typical Serial Tools Application

You can configure multiple Serial Analysis tools in series. An example of this would be in an RS-232C application where two computers are communicating with each other using a modem. Here you would use one tool to strip off the start bit, parity bit, and stop bit, and use the second tool to search for frame start and end patterns.

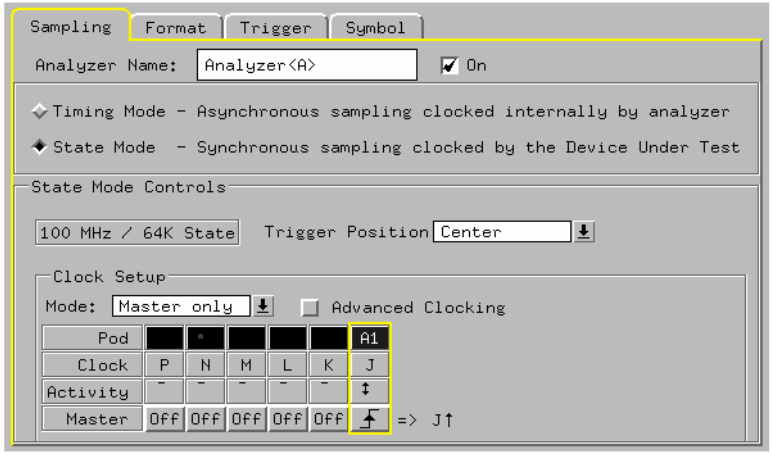


Logic Analyzer Configuration

How you configure the logic analyzer for a serial to parallel conversion may vary, however, in most cases the following configurations should be considered.

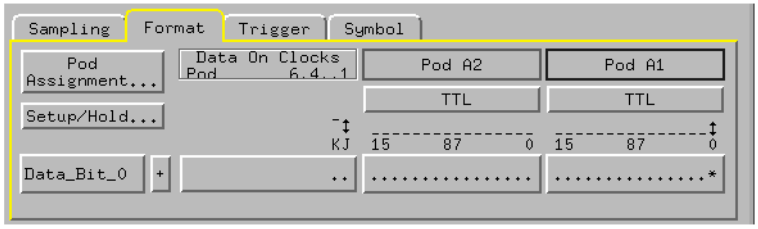
The Sampling Tab

Configure the *Sampling* window as shown below.



The Format Tab

Configure the *Format* window as shown below.

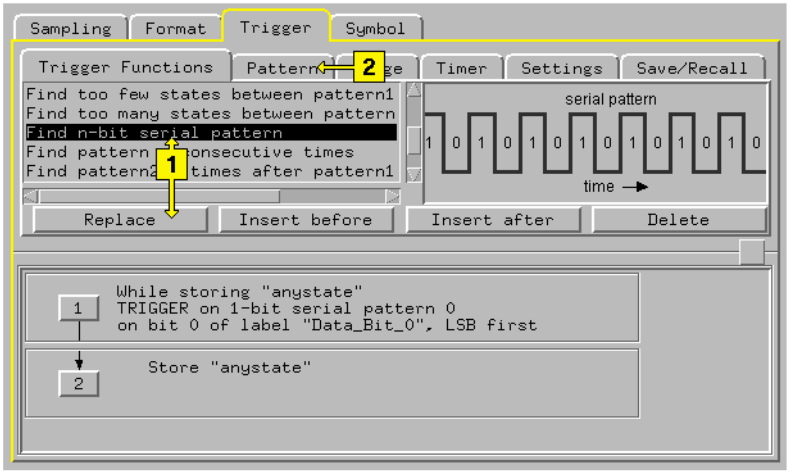


The Trigger Tab

1. Under the *Trigger Function* tab, select the macro *Find n-bit serial*

pattern, then select *Replace*.

2. Under the *Pattern* tab, set a serial pattern to trigger the analyzer.

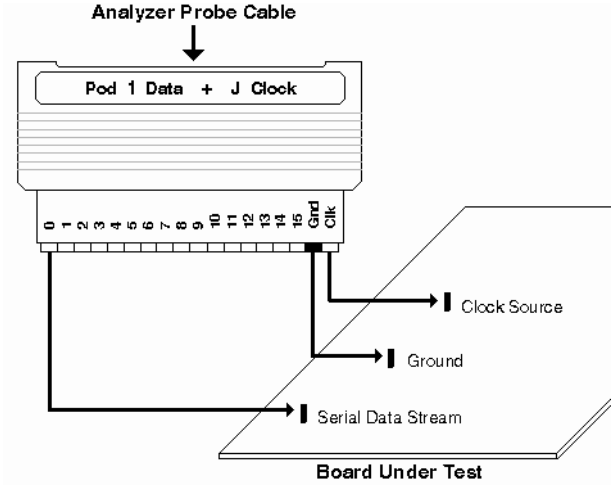


NOTE: For many applications, you can also use the "Find anystate n times" Trigger Macro.

Connect the Probing

In most cases, only one logic analyzer pod is required for a serial to parallel conversion. A single data channel is connected to the circuit trace where the serial data appears. If multiple clock signals are required in the master clock configuration, then multiple pods are required. Each pod has one clock channel available.

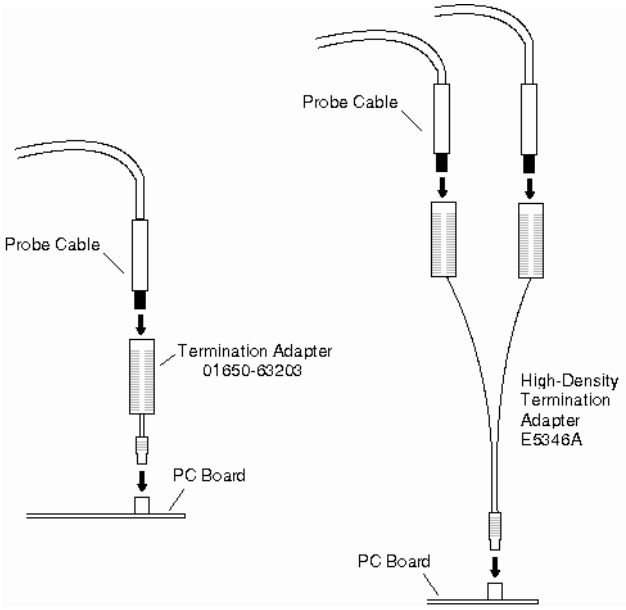
As far as the physical connection to the board, there are different methods used (see page 16) depending on the circuit. In the illustration below, the standard probe lead set is shown.



The standard lead set plugs directly into any .1-inch grid with 0.026 to 0.033-inch diameter round pins or 0.025-inch square pins. All probe tips work with 5059-4356 surface mount grabbers and 5959-0288 through-hole grabbers.

Probing Options

Direct Pod-to-Board Connection



Plug the termination adapters directly into the ©3M 2520-series, or similar alternative connector on the PC board.

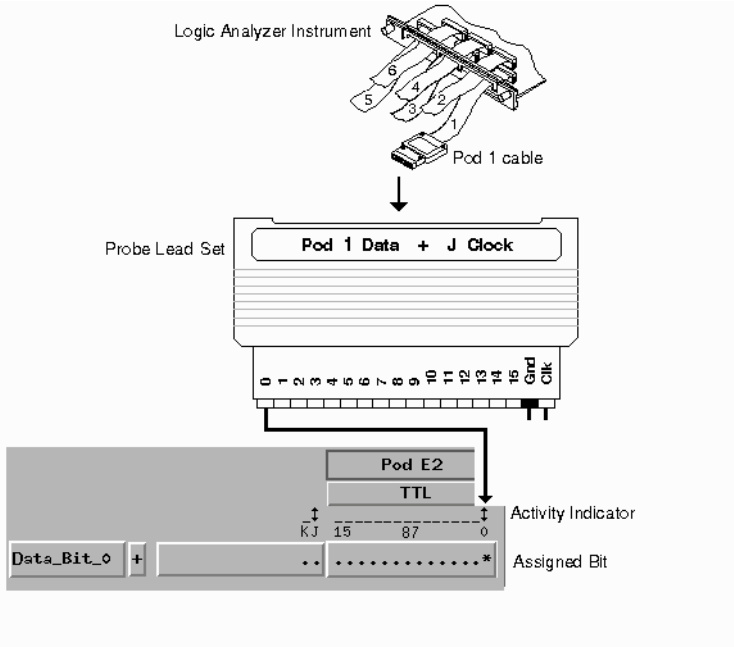
Mapping Probe Channels to the Interface

While the probes make the physical connection to your target circuit, a software connection is also made which routes the probed signals into the logic analyzer. This software connection is done in the Format window interface and is called signal-to-interface mapping.

The mapping process consists of logically grouping probed signals, with a similar identity or purpose, to a uniquely named label. To add or delete signals to a group, you simply assign bits (see page 18) under the label.

Example

The following example shows one probe channel (bit 0) on probe pod 1 mapped to one label (Data_Bit_0) in the Format window interface. When a bit is assigned, an asterisk "*" appears in the bit assignment field, verifying the software connection. You can also use the activity indicators to verify the probe connection to the circuit.



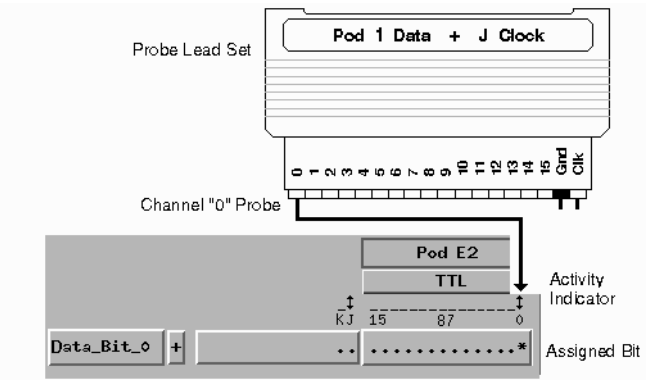
NOTE: After you set up your first measurement, use the ribbon cable ID clips to mark the data cable numbers for future reference.

Assigning Bits to a Label

The bits in a label correspond to the physical logic analyzer probe channels. When you run the logic analyzer, data is output on all bits (channels) that are assigned to labels. Unassigned bits are inactive.

An asterisk "*" indicates an assigned bit.

A period "." indicates an unassigned bit.



To Assign Bits

1. Select the bit assignment field to the right of the label name you want to define. Each bit assignment field corresponds to the data pod listed above it.
2. Select the bits you want to change, toggling them between an asterisk and a period.
3. When the bits are assigned as desired, close the dialog box.

NOTE: Select the bit assignment dialog to see a shortcut menu for assigning groups of bits.

Bits assigned to a label are numbered from right to left. The least significant assigned bit on the far right is numbered 0. The next assigned bit to the left is numbered 1, and so on. Labels can contain bits that are not consecutive; however, bits are always numbered consecutively within a label.

Loading or Saving Serial Analysis Configurations

Serial Analysis Tool settings can be saved to a configuration file along with the tools connected to it, and loaded from a previously saved configuration file.

- Loading Configuration Files (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume)
- Saving Configuration Files (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume)

NOTE:

The *Load Configuration* window can be accessed via File->Load Configuration.
The *Save Configuration* window can be accessed via File->Save Configuration.

Printing Serial Analysis Configurations and Data

The print windows operation prints just the Serial Analysis tool windows. Use this operation if you want a hardcopy or electronic record of configurations of the Serial Analysis main window or sub-windows.

NOTE: Only the main Serial Analysis tool window has the ability to initiate a print window function (File - Print This Window).

Printing the Main Window

1. Optional - configure the Print Options (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume) if desired. Print Options include print destination, file format type, filename autoincrement, and color/b&w; pixel mapping.
2. In the Serial Analysis tool menu bar, select *File*, then select *Print This Window*.

Printing the Sub-windows

1. Optional - configure the Print Options (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume) if desired. Print Options include print destination, file format type, filename autoincrement, and color/b&w; pixel mapping.
2. Resize the main window slightly larger than the sub-window, then move the sub-window on top and just below the main window menu bar.
3. In the Serial Analysis tool menu bar, select *File*, then select *Print This Window*.

See Also

Print Options (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume)

Printer Setup (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume)

Enable Frame Processing - Synchronized Conversions

You can configure a serial to parallel conversion to start and stop at specified bit patterns in the serial data stream. You do this by defining a frame of data with a start point and an end point. The start point is a user-defined bit pattern and the end point can be either another bit pattern or a selected number of bits.

Once a frame is defined, you have the option to process and view the data in that frame. When you *Enable frame processing*, a new start label is inserted into the Listing display that show the start point of the defined frame. If an end pattern is defined, an end label is also inserted into the Listing display.

Framing data is very useful if you want to synchronize the start of a serial to parallel conversion to a specific pattern of bits, and have the conversion end with a specific pattern of bits or after a data block of a specified length.

NOTE: If a defined frame is seen multiple times in a serial data stream, all instances are converted.

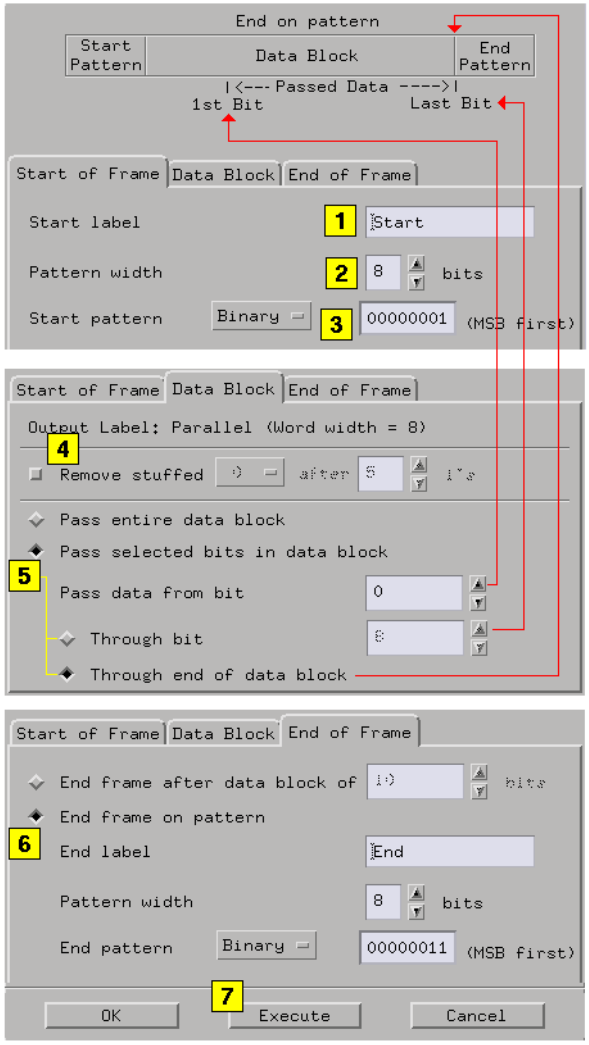
The following procedure begins from a basic serial analysis configuration. If you need to see an example of a serial to parallel conversion, refer to Example - Using the Serial Analysis Tool (see page 7).

Defining a Frame of Data

1. From the *Define Frame* dialog, enter a label name that identifys the start of the frame.
2. Define the bit width of the pattern.
3. Define the start of frame pattern.
4. Optional - If you want to remove a "stuffed bit", designate the number of 1's that precede the stuffed 0 bit.
5. Optional - If you want to convert all data in the frame, select *Pass entire*

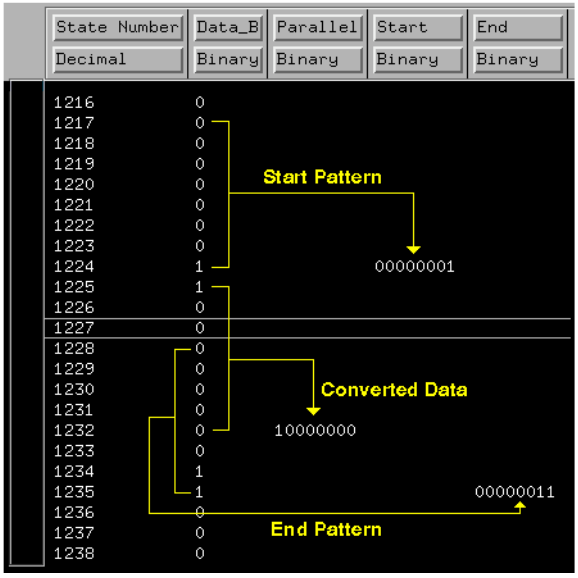
data block. If you only want to pass selected bits, or align the data on a first bit, define the first and last bit.

6. If you want the end of frame to occur after a certain number of bits, enter the bit number. If you want the frame of data to end when a pattern of bits occurs, specify the frame to end on a pattern. Configure the end pattern name, bit width and bit pattern as you did for the start pattern.
7. Select *Execute*.
   - Any time you change the configuration, re-execute the conversion.
   - If you want new serial data, re-run the analyzer.



Example Display

The following Listing display shows the results of the frame defined above. To make your listing look exactly like the example below, you may have to adjust the column width (see the *Listing Display Tool* help volume) and rearrange the label order (see the *Listing Display Tool* help volume).



If the defined frame is seen multiple times in the serial data stream, all instances are converted. If your conversion requires a starting point on a specific serial bit, define a beginning sample (see page 49).

Clock Recovery - Serial Data without a Clock

Clock Recovery is a process used when incoming serial data has no clock reference. Since the data has no clock, it is captured in timing analysis mode using the internal timing analyzer clock as the clock reference.

NOTE: For best results, the sample period of the Timing analyzer should be set so 4 or more sample points are taken on each serial bit.

The bit time of the serial data is set in the Clock Recovery dialog. The bit time is equal to:

```
1 / Bit Rate or 1 / Baud Rate
```

The serial data is sampled in the middle of each bit, and data edges are used to re-sync the sampling.

The bit time can be any number. It doesn't have to be a multiple of the timing analyzer clock. An internal bit clock is maintained in software and is re-synchronized on an edge. The first sampling point after an edge is at half the bit time from the edge, and successive points are sampled at intervals of the bit time. The sampled points are taken from the timing analyzer points that are closest to the ideal sample times of the internal bit clock.

If the Clock Recovery function is enabled, the incoming serial data is first sampled before the other serial analysis functions are performed. The sampled data is displayed under the label defined in the Clock Recovery dialog.

Considerations When Performing Clock Recovery

- Determine the Bit Time of the incoming serial data. Use the formula:

```
Bit Time = 1 / Bit Rate
```

- Use the logic analyzer in Timing mode.
- Set the timing analyzer Sample Period to:

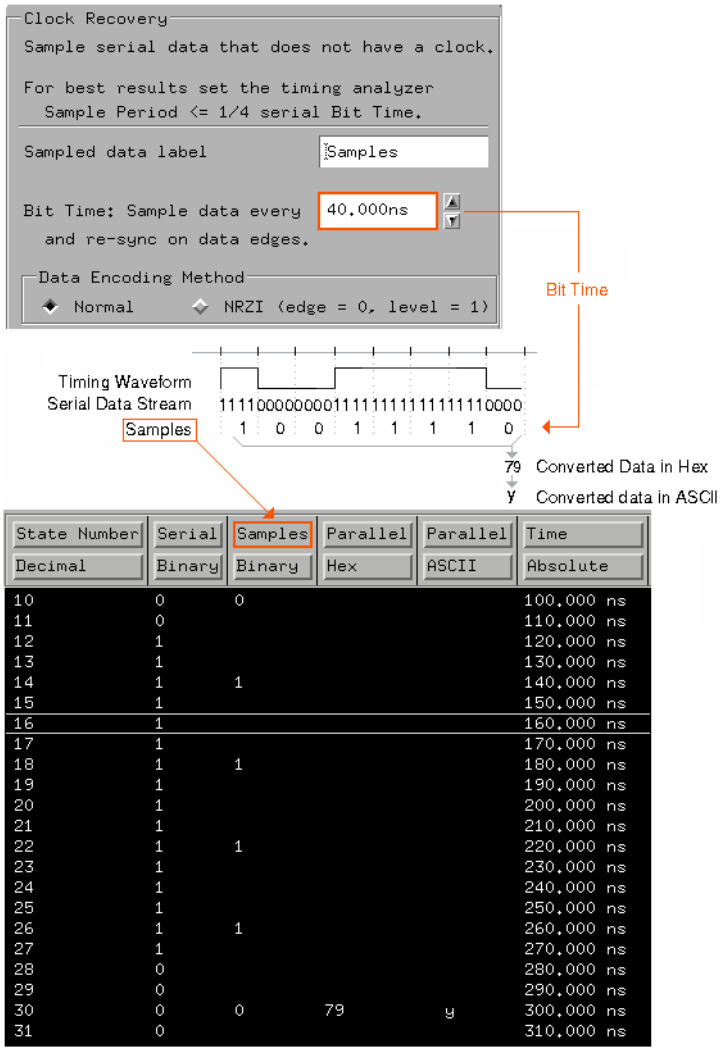
```
<= 1/4 of the Bit Time
```

- Any time you change the configuration, select *Execute Serial Analysis*.
- If you want new serial data, select the *Run Repetitive* icon.

NOTE: When Clock Recovery is turned on, the serial data generated under the "Sampled data label" in the Clock Recovery dialog becomes the serial data source that is converted.

The following illustration shows a Clock Recovery configuration with relation to a timing diagram and listing (last 21 bits) of a serial data stream that represents the ASCII letter *y* (LSB first format).

To make your listing look exactly like the example below, you may have to adjust the column width (see the *Listing Display Tool* help volume) and rearrange the label order (see the *Listing Display Tool* help volume).



Data Encoding Method

NRZ (Non-Return to Zero) encoding of serial data, also known as *Normal* is high for a "1" and low for a "0".

In contrast, for NRZI (Non-Return to Zero Inverted) encoding, also known as differential encoding, the signal level changes when a "0" occurs, whereas a "1" does not cause a change. For example, a stream

of 0's encoded in NRZI looks like a square wave. The signal changes on every bit.

Analyzing RS-232C Data

The following example analyzes serial data from an RS-232C output port for the purpose of verifying a *Print Screen* function. The intent of this example is to give you a conceptual view of using the Serial Analysis tool for similar measurements.

RS-232C Characteristics

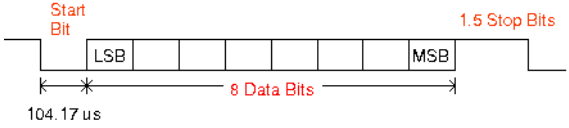
The characteristics for the RS-232C line in this example are as follows:

Bit Rate = 9600 Baud (9600 bits/sec.).

Voltage = -6 Volts to +6 Volts, inverted data.

Data Format = 1 start bit, 8 data bits, and 1.5 stop bits. Parity off.

The timing for RS-232C data before it is inverted is shown below.



Measurement Setup

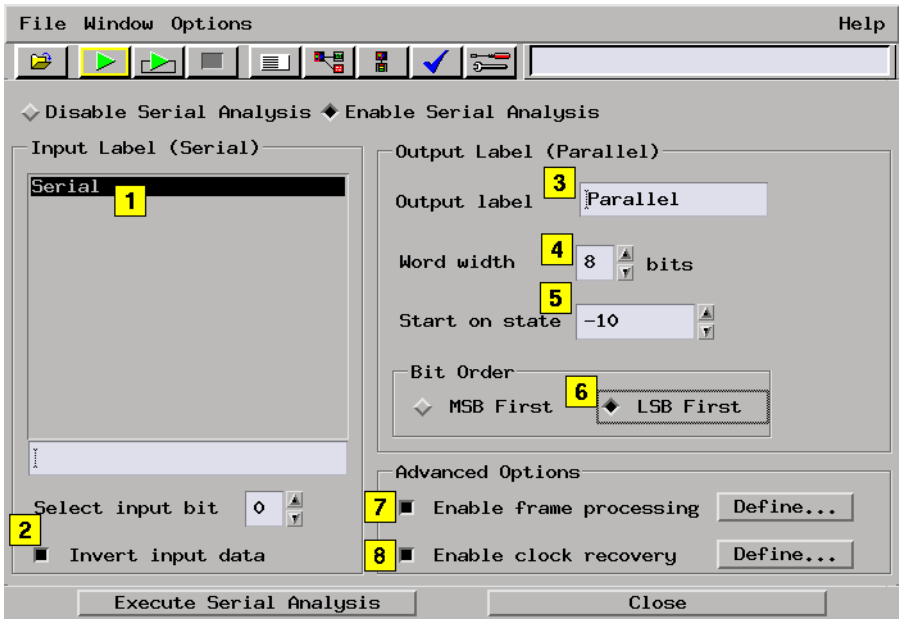
1. Configure the measurement (see page 34) with the appropriate tools.
2. Configure the logic analyzer (see page 35).
3. Connect the probing (see page 32) to your target circuit and map the probe channels (see page 33) into the Format tab of the logic analyzer.
4. Run the measurement to verify a trigger and data acquisition. This will also update the label list in the Serial Analysis window to include the new *Serial* label name in the analyzer.

Applying Serial Analysis to the RS-232C Data

From the Serial Analysis window, configure the tool as follows:

1. Select the *Serial* input label. If the *Serial* label does not appear in the label list, run the analyzer to register the new label.

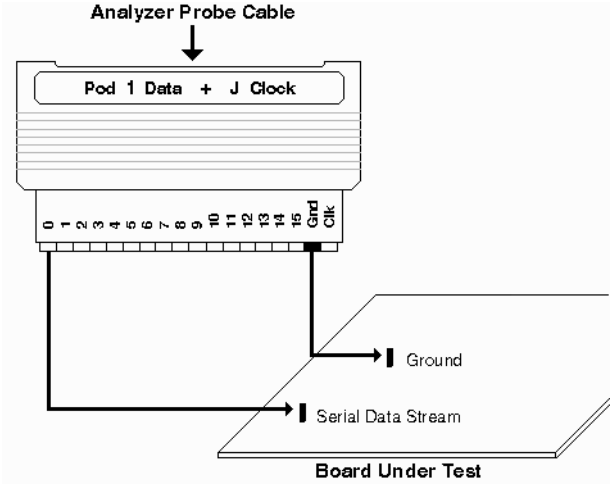
2. Invert the input data.
3. Optional - enter a new output label name. The default is *Parallel*.
4. Assign an 8 bit width to the new parallel word.
5. Set the conversion to *Start on state* -10.
6. Set the *Bit Order* so the new parallel word has the least significant bit (LSB) first.
7. Select *Enable frame processing*, then select *Define* to define the Frame parameters. (see page 37)
8. Select *Enable clock recovery*, then select *Define* to define the Clock Recovery. (see page 38)
9. Select the *Run* icon to acquire the serial data stream and execute the serial analysis.
10. View the results (see page 39) in the Listing Display tool.
11. Optional - place a marker (see page 40) on the *Start of Frame* pattern. This allows you to increment or decrement through all found frames.
12. Optional - compress (see page 41) the displayed data. This allows you to view only the data you want to see.



Connecting to Serial Data

NOTE: The following connection scheme is conceptual and should be changed according to your specific application.

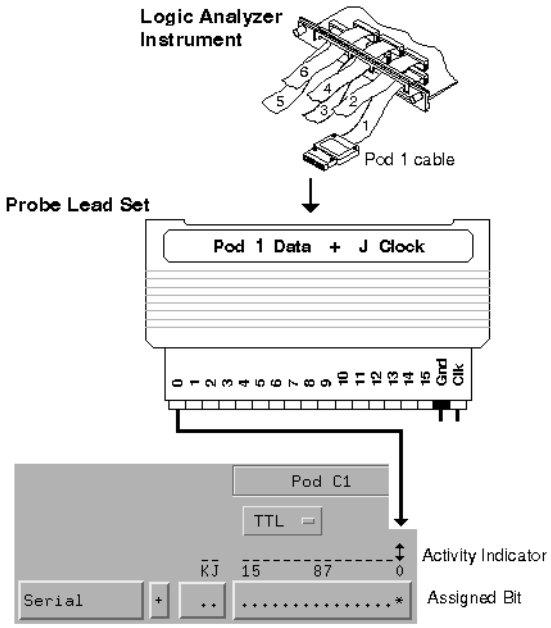
In most cases, only one logic analyzer pod is required for a serial to parallel conversion. A single data channel is connected to the circuit trace where the serial data appears.



The standard lead set plugs directly into any .1-inch grid with 0.026 to 0.033-inch diameter round pins or 0.025-inch square pins. All probe tips work with 5059-4356 surface mount grabbers and 5959-0288 through-hole grabbers.

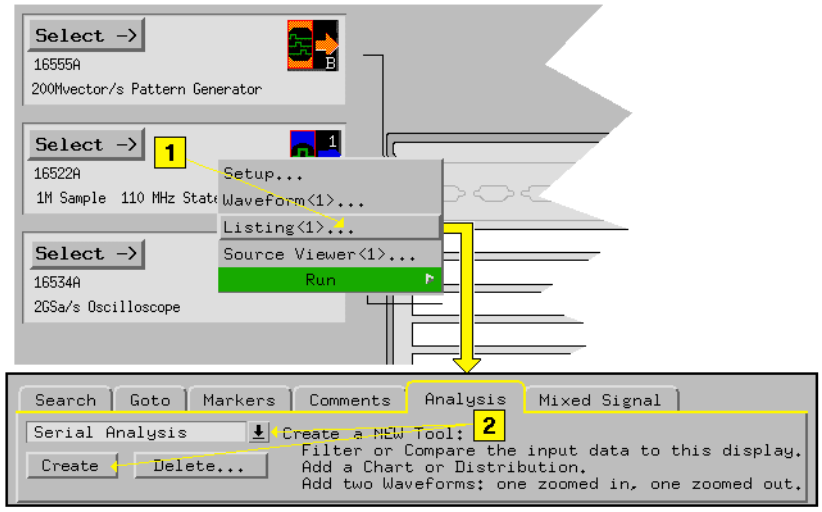
Map the Probe Channels

The map of the probe channel to the interface is shown below.



Configure the Measurement Tools

1. From the main *Logic Analysis System* window, select the logic analyzer icon, then select the *Listing* display. At this time, the Listing display window appears.
2. From the *Analysis* tab in the Listing display, select the *Serial Analysis* tool, then select *Create*. At this time the Serial Analysis window appears.

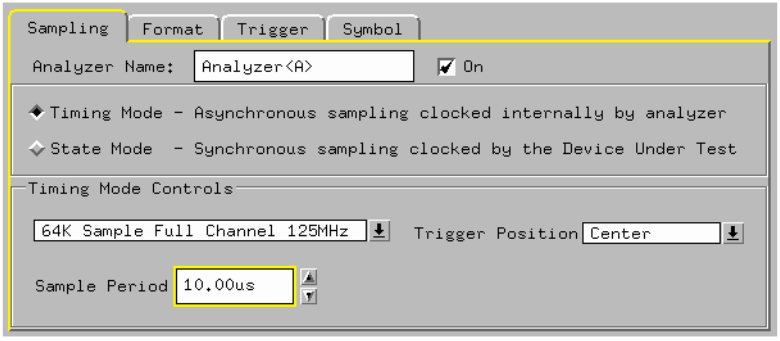


Analyzer Configuration

To access the logic analyzer configuration tabs, select logic analyzer tool icon in the main *Logic Analysis System* window, then select *Setup*.

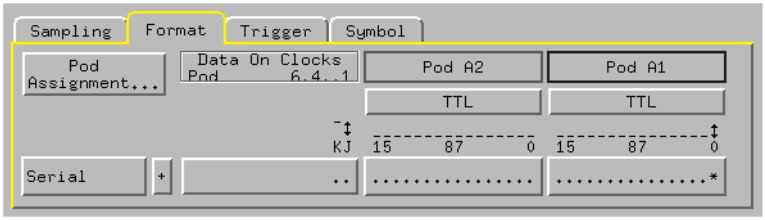
The Sampling Tab

Configure the *Sampling* window as shown below.



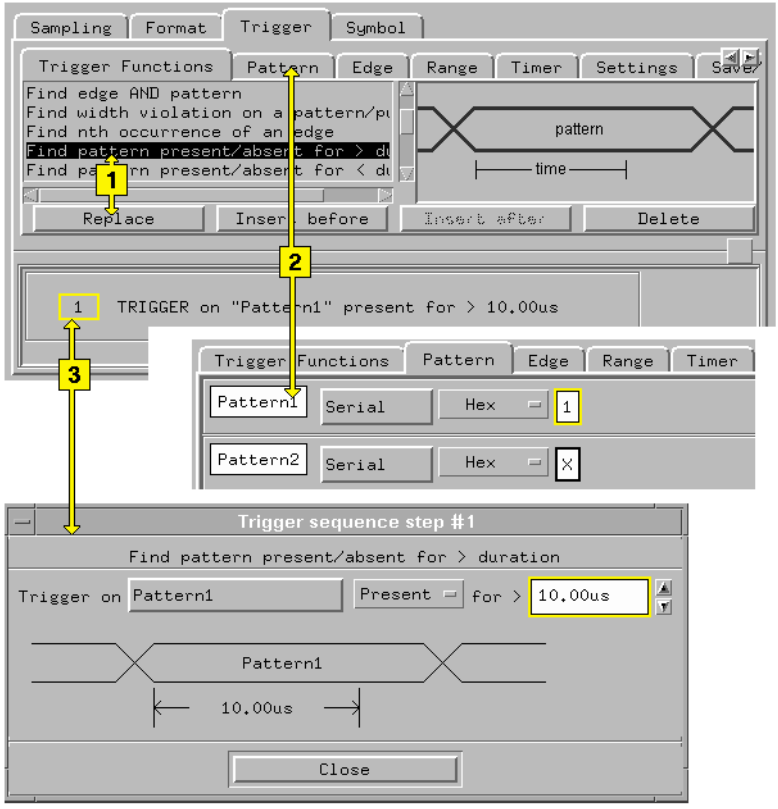
The Format Tab

Configure the *Format* window as shown below.



The Trigger Tab

1. From the *Trigger Function* tab select *find pattern present/absent for > duration*, then select *Replace*.
2. From the *Pattern* tab set a pattern of *1* and a duration of *10 us*.
3. Edit Sequence Level 1 to a duration of 10 us.

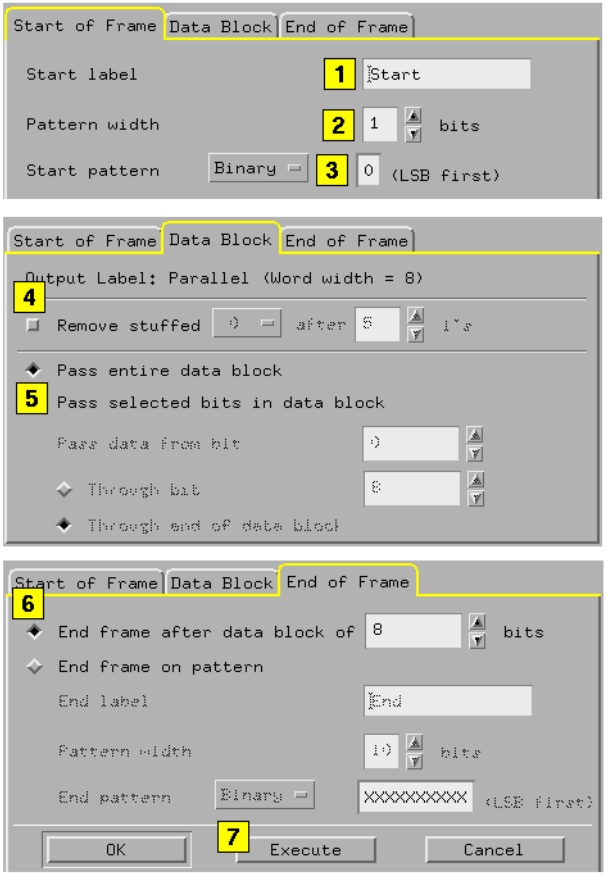


Define the Frame Parameters

Defining a Frame of Data

1. Optional - enter a new start label name. The default is *Start*.
2. Set the pattern width to 1 bit.
3. Define the pattern as a Binary 0.
4. Disable the *Remove Stuffed O* function.
5. Select *Pass entire data block*.
6. Set the end of frame to occur after a data block of 8 bits.

7. Select *Execute*.

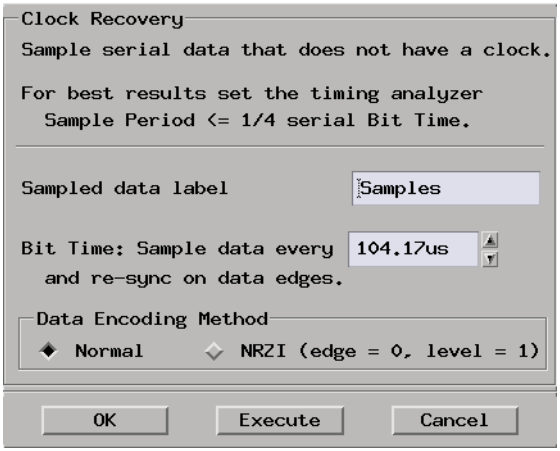


See Also Enable Frame Processing - Synchronized Conversions (see page 22)

Define the Clock Recovery

1. Optional - enter a new label name for the sample points. The default is *Samples*.
2. Set the *Bit Time* to 104.17 us. This is 1/bit rate = 1/9600 bits/sec.
3. Set Data Encoding Method to *Normal*.

4. Select *OK*.

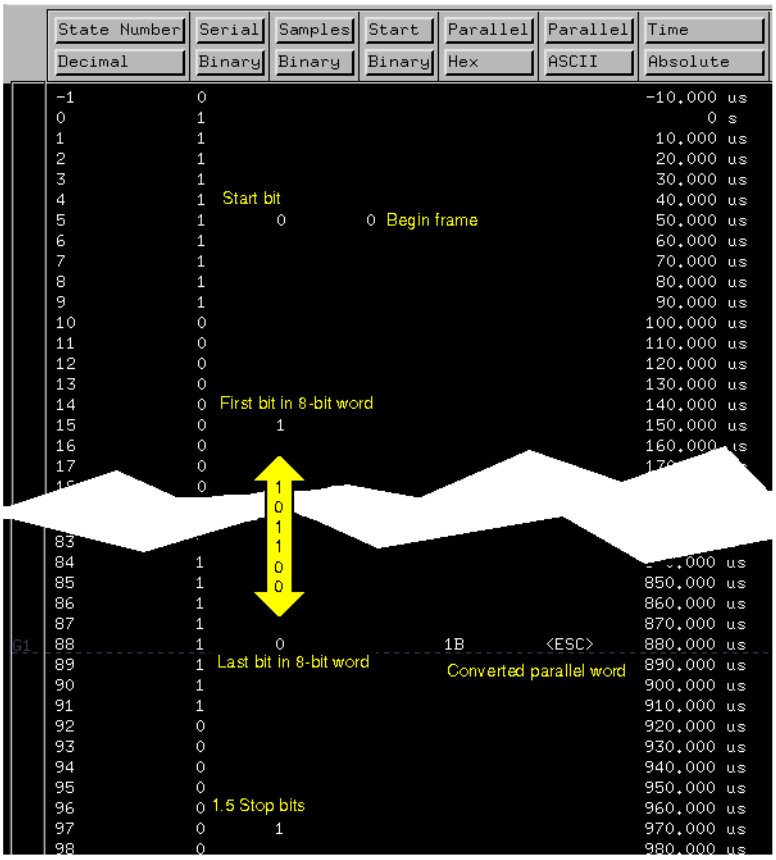


See Also Basics of Clock Recovery (see page 26)

Viewing the Results

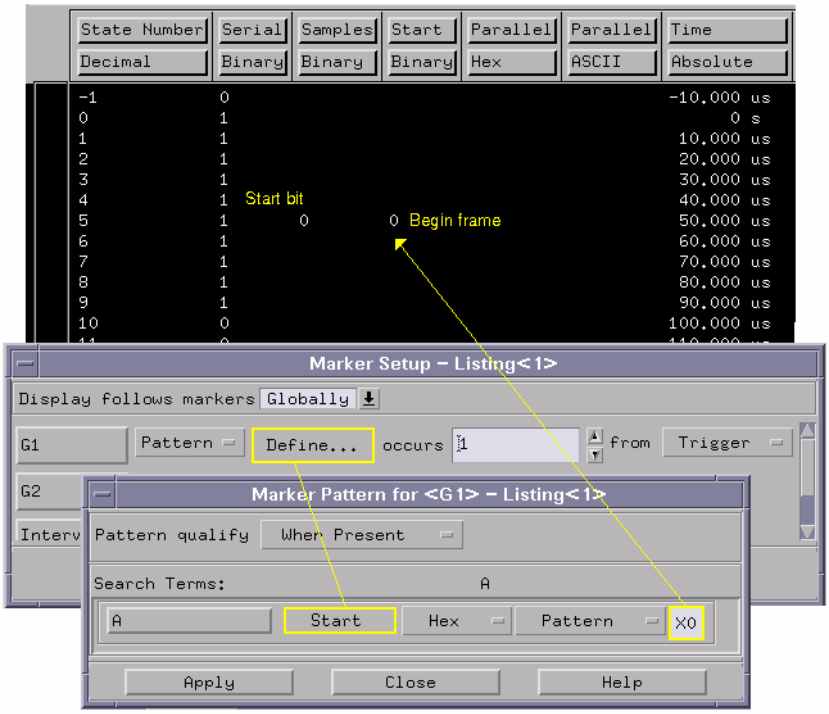
After you select the *Run All* icon, the results of the measurement appear in the Listing Display tool. To make your listing look exactly like the example below, you may have to adjust the column width (see the *Listing Display Tool* help volume) and rearrange the label order (see the *Listing Display Tool* help volume).

NOTE: Because of the length of the listing, only a beginning and ending segment is shown. To more easily view the important data, refer to Compressing the Displayed Data (see page 41)



Placing Markers on Converted Patterns

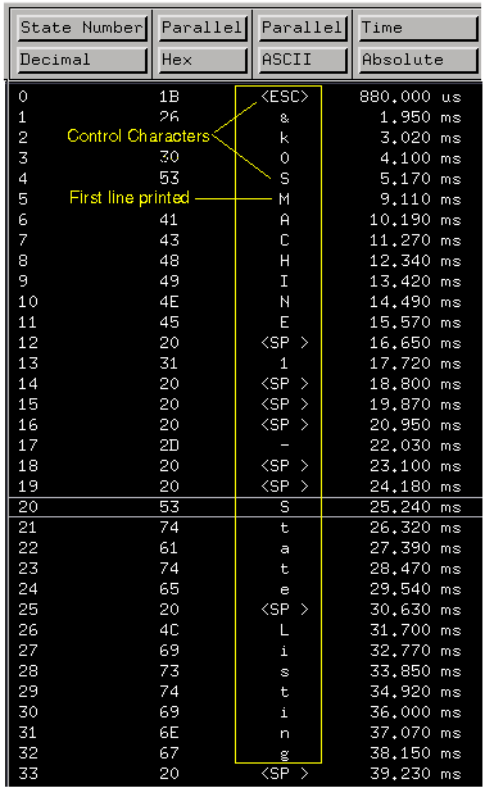
By placing a pattern marker (see the *Markers* help volume) on the *Start of Frame* pattern, you can search for the start of each frame or count frame occurrences.



Compressing the Displayed Data

To compress the data into a view that allows you to see just the important data, simply remove the unnecessary labels from the listing. The figure below shows only the converted parallel words and the parallel state numbers.

The first five characters ESC, &, K, O, and S, in the listing are control characters to the printer. The first line sent to the printer in this example is "MACHINE 1 - State Listing".



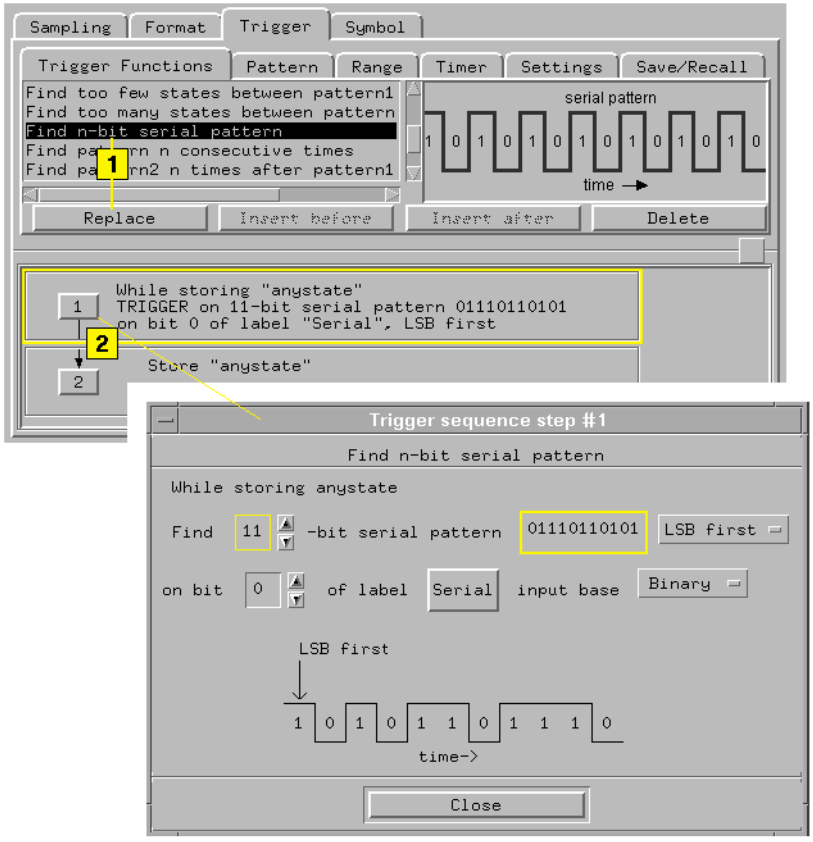
State Number Decimal	Parallel Hex	Parallel ASCII	Time Absolute
0	1B	<ESC>	880.000 us
1	26	&	1.950 ms
2	6B	k	3.020 ms
3	30	0	4.100 ms
4	53	S	5.170 ms
5	4D	M	9.110 ms
6	41	A	10.190 ms
7	43	C	11.270 ms
8	48	H	12.340 ms
9	49	I	13.420 ms
10	4E	N	14.490 ms
11	45	E	15.570 ms
12	20	<SP >	16.650 ms
13	31	1	17.720 ms
14	20	<SP >	18.800 ms
15	20	<SP >	19.870 ms
16	20	<SP >	20.950 ms
17	2D	-	22.030 ms
18	20	<SP >	23.100 ms
19	20	<SP >	24.180 ms
20	53	S	25.240 ms
21	74	t	26.320 ms
22	61	a	27.390 ms
23	74	t	28.470 ms
24	65	e	29.540 ms
25	20	<SP >	30.630 ms
26	4C	L	31.700 ms
27	69	i	32.770 ms
28	73	s	33.850 ms
29	74	t	34.920 ms
30	69	i	36.000 ms
31	6E	n	37.070 ms
32	67	g	38.150 ms
33	20	<SP >	39.230 ms

Triggering on a Serial Pattern

In the State mode of many logic analyzers you have the capability to trigger on 11-bit serial patterns by using the "Find n-bit serial pattern" trigger macro. From the *Trigger* window, select the macro as follows:

1. From the *Trigger Functions* tab, select *Find n-bit serial pattern*, then select *Replace*.
2. Select Sequence Level 1, then configure the macro parameters as required by your application.

NOTE: If the actual start pattern is longer than 11 bits, you still may trigger with only occasionally false triggers, by specifying just the last 11 bits.



In the timing mode there are several ways to specify a trigger. If the start of the serial transmission can be controlled, the trigger can be set to the first occurrence of an edge in the serial data.

If the serial data is continuously transmitted, the easiest method is to trigger on any edge and let the Serial Analysis tool find the first start pattern. With deep memory, triggering on a start of frame is usually not an issue since many frames of data are captured.

A second method is the use of the trigger macro *Find pattern present/absent for > duration*. Some serial protocols such as the CAN bus have idle periods where the data line goes high for a certain minimum period of time.

A third method is to trigger on an external event that indicates the

beginning of a frame of data.

Using Markers to Find Frames

A useful feature in the Listing Display tool for doing serial analysis is the Pattern marker. For example, by assigning a Pattern marker the same bit pattern as the *Start of frame*, you can then increment or decrement through all occurrences of that frame.

In general, searching and marking data patterns is a post-processing task done after a serial to parallel conversion is executed and the converted data is displayed in the Listing Display tool.

For more information on placing Pattern markers in data, refer to Placing Pattern Markers (see the *Markers* help volume).

Selecting the Input Label

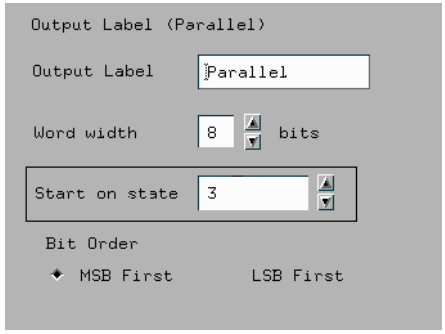
The input label you select is one of the predefined labels in the logic analyzer Format window. If labels are not created and given assigned bits in the Format window, they do not appear in the list of Input labels.

Setting Significant Bit order

Use the Bit Order selection to specify the order in which the bits occur in the serial data stream. Select *MSB First* if the MSB (most significant bit) occurs before the LSB (least significant bit) in the serial data stream. Select *LSB First* if the LSB occurs first.

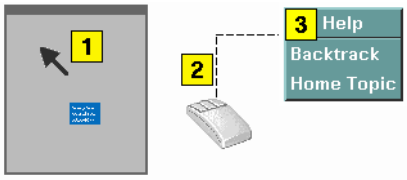
Beginning Sample

The *Start on state* control specifies the serial bit where the parallel conversion begins. This can be useful for aligning words on a desired bit in the parallel word.



Help - How to Navigate Quickly

1. Place mouse cursor anywhere in a help window.
2. Press the right mouse button.
3. Select desired destination.



You can also access all navigation and search commands from the help window menu bar.

Help - System Overview

The help system is divided into *System* Help, and *Tool* Help. All help is designed to be task oriented and specific to the window where tasks are performed.

Links, in most cases, are confined to topics in the specific window where help was requested. However, some links do go up to system-level topics from specific tool windows. When this occurrs, a second help window will appear. Since the definition of future tools is hard to link to, there are no links going from the system level down to specific tools.

System Help

The system help is accessed through the *Help* field in the menu bar of the main system window. It offers help on system-level topics and operations.

Tool Help

As you add new software and hardware tools to the system, the tool specific help is added. Tool specific help is accessed through the *Help* field in the menu bar of the specific tool windows.

Using Help

In addition to system and tool help, there is help on help called *Using Help*. Using Help shows you how to navigate and search the help systems and to print help topics. Using Help is accessed through the *Help* field in all windows.

absolute Denotes the time period or count of states between a captured state and the trigger state. An absolute count of -10 indicates the state was captured ten states before the trigger state was captured.

acquisition Denotes one complete cycle of data gathering by a measurement module. For example, if you are using an analyzer with 128K memory depth, one complete acquisition will capture and store 128K states in acquisition memory.

analysis probe A probe connected to a microprocessor or standard bus in the device under test. An analysis probe provides an interface between the signals of the microprocessor or standard bus and the inputs of the logic analyzer. Also called a *preprocessor*.

analyzer 1 In a logic analyzer with two *machines*, refers to the machine that is on by default. The default name is *Analyzer<N>*, where N is the slot letter.

analyzer 2 In a logic analyzer with two *machines*, refers to the machine that is off by default. The default name is *Analyzer<N2>*, where N is the slot letter.

arming An instrument tool must be armed before it can search for its trigger condition. Typically, instruments are armed immediately when *Run* or *Group Run* is selected. You can set up one instrument to arm another using the *Intermodule Window*. In these setups, the second instrument cannot search for its trigger condition until it receives the arming signal from the first instrument. In some analyzer instruments, you can set up one analyzer *machine* to arm the other analyzer machine in the *Trigger Window*.

asterisk (*) See *edge terms*, *glitch*, and *labels*.

bits Bits represent the physical logic analyzer channels. A bit is a *channel* that has or can be assigned to a *label*. A bit is also a position in a label.

card This refers to a single instrument intended for use in the Agilent Technologies 16700A/B-series mainframes. One card fills one slot in the mainframe. A module may comprise a single card or multiple cards cabled together.

channel The entire signal path from the probe tip, through the cable and module, up to the label grouping.

click When using a mouse as the

pointing device, to click an item, position the cursor over the item. Then quickly press and release the *left mouse button*.

clock channel A logic analyzer *channel* that can be used to carry the clock signal. When it is not needed for clock signals, it can be used as a *data channel*, except in the Agilent Technologies 16517A.

context record A context record is a small segment of analyzer memory that stores an event of interest along with the states that immediately preceded it and the states that immediately followed it.

context store If your analyzer can perform context store measurements, you will see a button labeled *Context Store* under the Trigger tab. Typical context store measurements are used to capture writes to a variable or calls to a subroutine, along with the activity preceding and following the events. A context store measurement divides analyzer memory into a series of context records. If you have a 64K analyzer memory and select a 16-state context, the analyzer memory is divided into 4K 16-state context records. If you have a 64K analyzer memory and select a 64-state context, the analyzer memory will be divided into 1K 64-state records.

count The count function records periods of time or numbers of state transactions between states stored in memory. You can set up the analyzer count function to count occurrences of a selected event during the trace, such as counting how many times a variable is read between each of the writes to the variable. The analyzer can also be set up to count elapsed time, such as counting the time spent executing within a particular function during a run of your target program.

cross triggering Using intermodule capabilities to have measurement modules trigger each other. For example, you can have an external instrument arm a logic analyzer, which subsequently triggers an oscilloscope when it finds the trigger state.

data channel A *channel* that carries data. Data channels cannot be used to clock logic analyzers.

data field A data field in the pattern generator is the data value associated with a single label within a particular data vector.

data set A data set is made up of all labels and data stored in memory of any single analyzer machine or

instrument tool. Multiple data sets can be displayed together when sourced into a single display tool. The Filter tool is used to pass on partial data sets to analysis or display tools.

debug mode See *monitor*.

delay The delay function sets the horizontal position of the waveform on the screen for the oscilloscope and timing analyzer. Delay time is measured from the trigger point in seconds or states.

demo mode An emulation control session which is not connected to a real target system. All windows can be viewed, but the data displayed is simulated. To start demo mode, select *Start User Session* from the Emulation Control Interface and enter the demo name in the *Processor Probe LAN Name* field. Select the *Help* button in the *Start User Session* window for details.

deskewing To cancel or nullify the effects of differences between two different internal delay paths for a signal. Deskewing is normally done by routing a single test signal to the inputs of two different modules, then adjusting the Intermodule Skew so that both modules recognize the signal at the same time.

device under test The system under test, which contains the circuitry you are probing. Also known as a *target system*.

don't care For *terms*, a "don't care" means that the state of the signal (high or low) is not relevant to the measurement. The analyzer ignores the state of this signal when determining whether a match occurs on an input label. "Don't care" signals are still sampled and their values can be displayed with the rest of the data. Don't cares are represented by the *X* character in numeric values and the dot (.) in timing edge specifications.

dot (.) See *edge terms*, *glitch*, *labels*, and *don't care*.

double-click When using a mouse as the pointing device, to double-click an item, position the cursor over the item, and then quickly press and release the *left mouse button* twice.

drag and drop Using a Mouse: Position the cursor over the item, and then press and hold the *left mouse button*. While holding the left mouse button down, move the mouse to drag the item to a new location. When the item is positioned where you want it, release the mouse button.

Using the Touchscreen:
Position your finger over the item, then press and hold finger to the screen. While holding the finger down, slide the finger along the screen dragging the item to a new location. When the item is positioned where you want it, release your finger.

edge mode In an oscilloscope, this is the trigger mode that causes a trigger based on a single channel edge, either rising or falling.

edge terms Logic analyzer trigger resources that allow detection of transitions on a signal. An edge term can be set to detect a rising edge, falling edge, or either edge. Some logic analyzers can also detect no edge or a *glitch* on an input signal. Edges are specified by selecting arrows. The dot (.) ignores the bit. The asterisk (*) specifies a glitch on the bit.

emulation module A module within the logic analysis system mainframe that provides an emulation connection to the debug port of a microprocessor. An E5901A emulation module is used with a target interface module (TIM) or an analysis probe. An E5901B emulation module is used with an E5900A emulation probe.

emulation probe The stand-alone equivalent of an *emulation module*. Most of the tasks which can be performed using an emulation module can also be performed using an emulation probe connected to your logic analysis system via a LAN.

emulator An *emulation module* or an *emulation probe*.

Ethernet address See *link-level address*.

events Events are the things you are looking for in your target system. In the logic analyzer interface, they take a single line. Examples of events are *Label1 = XX* and *Timer 1 > 400 ns*.

filter expression The filter expression is the logical *OR* combination of all of the filter terms. States in your data that match the filter expression can be filtered out or passed through the Pattern Filter.

filter term A variable that you define in order to specify which states to filter out or pass through. Filter terms are logically OR'ed together to create the filter expression.

Format The selections under the logic analyzer *Format* tab tell the

logic analyzer what data you want to collect, such as which channels represent buses (labels) and what logic threshold your signals use.

frame The Agilent Technologies or 16700A/B-series logic analysis system mainframe. See also *logic analysis system*.

gateway address An IP address entered in integer dot notation. The default gateway address is 0.0.0.0, which allows all connections on the local network or subnet. If connections are to be made across networks or subnets, this address must be set to the address of the gateway machine.

glitch A glitch occurs when two or more transitions cross the logic threshold between consecutive timing analyzer samples. You can specify glitch detection by choosing the asterisk (*) for *edge terms* under the timing analyzer Trigger tab.

grouped event A grouped event is a list of *events* that you have grouped, and optionally named. It can be reused in other trigger sequence levels. Only available in Agilent Technologies 16715A or higher logic analyzers.

held value A value that is held until the next sample. A held value can exist in multiple data sets.

immediate mode In an oscilloscope, the trigger mode that does not require a specific trigger condition such as an edge or a pattern. Use immediate mode when the oscilloscope is armed by another instrument.

interconnect cable Short name for *module/probe interconnect cable*.

intermodule bus The intermodule bus (IMB) is a bus in the frame that allows the measurement modules to communicate with each other. Using the IMB, you can set up one instrument to *arm* another. Data acquired by instruments using the IMB is time-correlated.

intermodule Intermodule is a term used when multiple instrument tools are connected together for the purpose of one instrument arming another. In such a configuration, an arming tree is developed and the group run function is designated to start all instrument tools. Multiple instrument configurations are done in the Intermodule window.

internet address Also called Internet Protocol address or IP address. A 32-bit network address. It

is usually represented as decimal numbers separated by periods; for example, 192.35.12.6. Ask your LAN administrator if you need an internet address.

labels Labels are used to group and identify logic analyzer channels. A label consists of a name and an associated bit or group of bits. Labels are created in the Format tab.

line numbers A line number (Line #s) is a special use of *symbols*. Line numbers represent lines in your source file, typically lines that have no unique symbols defined to represent them.

link-level address Also referred to as the Ethernet address, this is the unique address of the LAN interface. This value is set at the factory and cannot be changed. The link-level address of a particular piece of equipment is often printed on a label above the LAN connector. An example of a link-level address in hexadecimal: 0800090012AB.

local session A local session is when you run the logic analysis system using the local display connected to the product hardware.

logic analysis system The Agilent Technologies 16700A/B-series mainframes, and all tools designed to work with it. Usually used to mean the specific system and tools you are working with right now.

machine Some logic analyzers allow you to set up two measurements at the same time. Each measurement is handled by a different machine. This is represented in the Workspace window by two icons, differentiated by a *1* and a *2* in the upper right-hand corner of the icon. Logic analyzer resources such as pods and trigger terms cannot be shared by the machines.

markers Markers are the green and yellow lines in the display that are labeled *x*, *o*, *G1*, and *G2*. Use them to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of states in the data. The x and o markers are local to the immediate display, while G1 and G2 are global between time correlated displays.

master card In a module, the master card controls the data acquisition or output. The logic analysis system references the module by the slot in which the master card is plugged. For example, a 5-card Agilent Technologies 16555D would be referred to as *Slot C:*

machine because the master card is in slot C of the mainframe. The other cards of the module are called *expansion cards*.

menu bar The menu bar is located at the top of all windows. Use it to select *File* operations, tool or system *Options*, and tool or system level *Help*.

message bar The message bar displays mouse button functions for the window area or field directly beneath the mouse cursor. Use the mouse and message bar together to prompt yourself to functions and shortcuts.

module/probe interconnect cable

The module/probe interconnect cable connects an E5901B emulation module to an E5900B emulation probe. It provides power and a serial connection. A LAN connection is also required to use the emulation probe.

module An instrument that uses a single timebase in its operation. Modules can have from one to five cards functioning as a single instrument. When a module has more than one card, system window will show the instrument icon in the slot of the *master card*.

monitor When using the Emulation Control Interface, running the monitor means the processor is in debug mode (that is, executing the debug exception) instead of executing the user program.

panning The action of moving the waveform along the timebase by varying the delay value in the Delay field. This action allows you to control the portion of acquisition memory that will be displayed on the screen.

pattern mode In an oscilloscope, the trigger mode that allows you to set the oscilloscope to trigger on a specified combination of input signal levels.

pattern terms Logic analyzer resources that represent single states to be found on labeled sets of bits; for example, an address on the address bus or a status on the status lines.

period (.) See *edge terms*, *glitch*, *labels*, and *don't care*.

pod pair A group of two pods containing 16 channels each, used to physically connect data and clock signals from the unit under test to the analyzer. Pods are assigned by pairs in the analyzer interface. The number of pod pairs available is determined

by the channel width of the instrument.

pod See *pod pair*

point To point to an item, move the mouse cursor over the item, or position your finger over the item.

preprocessor See *analysis probe*.

primary branch The primary branch is indicated in the *Trigger sequence step* dialog box as either the *Then find* or *Trigger on* selection. The destination of the primary branch is always the next state in the sequence, except for the Agilent Technologies 16517A. The primary branch has an optional occurrence count field that can be used to count a number of occurrences of the branch condition. See also *secondary branch*.

probe A device to connect the various instruments of the logic analysis system to the target system. There are many types of probes and the one you should use depends on the instrument and your data requirements. As a verb, "to probe" means to attach a probe to the target system.

processor probe See *emulation probe*.

range terms Logic analyzer resources that represent ranges of values to be found on labeled sets of bits. For example, range terms could identify a range of addresses to be found on the address bus or a range of data values to be found on the data bus. In the trigger sequence, range terms are considered to be true when any value within the range occurs.

relative Denotes time period or count of states between the current state and the previous state.

remote display A remote display is a display other than the one connected to the product hardware. Remote displays must be identified to the network through an address location.

remote session A remote session is when you run the logic analyzer using a display that is located away from the product hardware.

right-click When using a mouse for a pointing device, to right-click an item, position the cursor over the item, and then quickly press and release the *right mouse button*.

sample A data sample is a portion of a *data set*, sometimes just one point. When an instrument samples the target system, it is taking a single

measurement as part of its data acquisition cycle.

Sampling Use the selections under the logic analyzer Sampling tab to tell the logic analyzer how you want to make measurements, such as State vs. Timing.

secondary branch The secondary branch is indicated in the *Trigger sequence step* dialog box as the *Else on* selection. The destination of the secondary branch can be specified as any other active sequence state. See also *primary branch*.

session A session begins when you start a *local session* or *remote session* from the session manager, and ends when you select *Exit* from the main window. Exiting a session returns all tools to their initial configurations.

skew Skew is the difference in channel delays between measurement channels. Typically, skew between modules is caused by differences in designs of measurement channels, and differences in characteristics of the electronic components within those channels. You should adjust measurement modules to eliminate as much skew as possible so that it does not affect the accuracy of your measurements.

state measurement In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are *synchronous* with the test system.

store qualification Store qualification is only available in a *state measurement*, not *timing measurements*. Store qualification allows you to specify the type of information (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as no-ops or wait-loops. To set up store qualification, use the *While storing* field in a logic analyzer trigger sequence dialog.

subnet mask A subnet mask blocks out part of an IP address so that the networking software can determine whether the destination host is on a local or remote network. It is usually represented as decimal numbers separated by periods; for example, 255.255.255.0. Ask your LAN administrator if you need a the subnet mask for your network.

symbols Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of symbols are available:

- Object file symbols - Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
- User-defined symbols - Symbols you create.

Symbols can be used as *pattern* and *range* terms for:

- Searches in the listing display.
- Triggering in logic analyzers and in the source correlation trigger setup.
- Qualifying data in the filter tool and system performance analysis tool set.

system administrator The system administrator is a person who manages your system, taking care of such tasks as adding peripheral devices, adding new users, and doing system backup. In general, the system administrator is the person you go to with questions about implementing your software.

target system The system under test, which contains the microprocessor you are probing.

terms Terms are variables that can be used in trigger sequences. A term can be a single value on a label or set of labels, any value within a range of values on a label or set of labels, or a glitch or edge transition on bits within a label or set of labels.

TIM A TIM (Target Interface Module) makes connections between the cable from the emulation module or emulation probe and the cable to the debug port on the system under test.

time-correlated Time correlated measurements are measurements involving more than one instrument in which all instruments have a common time or trigger reference.

timer terms Logic analyzer resources that are used to measure the time the trigger sequence remains within one sequence step, or a set of sequence steps. Timers can be used to detect when a condition lasts too long or not long enough. They can be used to measure pulse duration, or duration of a wait loop. A single timer term can be used to delay trigger until a period of time after detection of a significant event.

timing measurement In a timing measurement, the logic analyzer samples data at regular intervals according to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the system under test, timing measurements capture traces of electrical activity over time. These measurements are *asynchronous* with the test system.

tool icon Tool icons that appear in the workspace are representations of the hardware and software tools selected from the toolbox. If they are placed directly over a current measurement, the tools automatically connect to that measurement. If they are placed on an open area of the main window, you must connect them to a measurement using the mouse.

toolbox The Toolbox is located on the left side of the main window. It is used to display the available hardware and software tools. As you add new tools to your system, their icons will appear in the Toolbox.

tools A tool is a stand-alone piece of functionality. A tool can be an instrument that acquires data, a display for viewing data, or a post-processing analysis helper. Tools are represented as icons in the main window of the interface.

trace See *acquisition*.

trigger sequence A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to *trigger*.

trigger specification A trigger specification is a set of conditions that must be true before the instrument triggers.

trigger Trigger is an event that occurs immediately after the instrument recognizes a match between the incoming data and the trigger specification. Once trigger occurs, the instrument completes its *acquisition*, including any store qualification that may be specified.

workspace The workspace is the large area under the message bar and to the right of the toolbox. The workspace is where you place the different instrument, display, and analysis tools. Once in the workspace, the tool icons graphically represent a complete picture of the measurements.

zooming In the oscilloscope or timing analyzer, to expand and contract the waveform along the time base by varying the value in the s/Div

field. This action allows you to select specific portions of a particular waveform in acquisition memory that will be displayed on the screen. You can view any portion of the waveform record in acquisition memory.

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